



Bhattacharya 4-6-2

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

**Patent Application**

Applicant(s): D. Bhattacharya et al.  
Case: 4-6-2  
Serial No.: 10/776,778  
Filing Date: February 11, 2004  
Group: To Be Assigned  
Examiner: To Be Assigned

I hereby certify that this paper is being deposited on this date with the U.S. Postal Service as first class mail addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Signature: *Lisa L. Vulpis* Date: March 29, 2004

Title: Multiple Voltage Level Detection Circuit

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TRANSMITTAL OF FORMAL DRAWINGS

Mail Stop PGPUB Drawings  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Attention: Official Draftsperson

Sir:

Applicants submit herewith two (2) sheets of formal drawings in the above-referenced application.

Respectfully submitted,

Date: March 29, 2004

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